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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,303	10/24/2003	Norman Paul Jouppi	200301893-2	1502

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EXAMINER
MCLEAN MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,303	JOUPPI ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,10-13,19 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10-13,19,23 and 24* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on October 24, 2003 and the Information Disclosure Statement submitted on January 16, 2004.

Priority

2. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 119(a)-(d). This case is a continuation of U.S. Patent 6,665,776.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 11-13 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado et al. (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820).

Regarding claims 1 and 23, Lopez-Aguado discloses a processor having a normal mode (normal mode occurs during cache hits) and a speculative prefetching mode (speculative mode occurs during prefetch cache hits when the prefetch bit is not asserted and when data cache misses occur), the processor operable in the speculative prefetching mode after a data cache miss comprising a first data cache for storing data when the processor operates in the normal mode (Figure 3, Reference 105; C 6, L 57-60 – inherently data is stored in cache 105 when a cache write hit occurs); and a second data cache for storing data in response to a store instruction only

when the processor operates in the speculative prefetching mode (Figure 3, Reference 106; C 6, L 27-54; C 6, L 60-67; C 7, L 1-67); a first program counter for use when the processor operates in the normal mode (C 4, L 10-11; C 5, L 57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C 2, L 24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Regarding claim 2, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data (Lopez-Aguado - Figure 5, Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

Regarding claims 11-12 and 24, Lopez-Aguado discloses a processor having a normal mode and a speculative prefetching mode, wherein the processor operates in the speculative prefetching mode after a data cache miss occurs comprising a first register/first cache (a cache is random access memory comprised of registers, the first register consists of one of the registers in cache 105 in Figure 3) for storing data during the normal mode (normal mode occurs during data cache hits to Reference 105 of Figure 3; inherently data is stored in cache 105 when a cache write hit occurs); a second register/second data cache (the second register consists of one of the registers in cache 106 in Figure 3) for storing data only during the speculative prefetching mode (C 6, L 27-54; C 6, L 60-67; C 7, L 1-67; speculative prefetching mode occurs during prefetch cache hits when the PREFETCH bit is un-asserted [C 6, L 60-67; C 7, L 1-67] and after data cache misses [C 6, L 27-54] and data is stored in the second register only during the speculative prefetching mode), the second register comprising a first trash bit that indicates whether the second register contains arbitrary data (Figure 5, Reference INV); an instruction bus for receiving a stream of instructions including a first instruction and a second instruction (Figure 4, Reference 128; C 4, L 22-28); control logic for executing the first instruction (C 6, L 10-13 - primary pipeline for executing the first instruction having an un-asserted LP bit); control logic for initiating a cache fill request provided execution of the first instruction encounters a data cache miss (C 6, L 34-48); control logic for setting the trash bit of the second register in response to the first instruction and the data cache miss (C 6, L 34-54); control logic for executing the second instruction in the speculative prefetching mode using the second register in place of the first register (C 4, L 22-34; C 5, L 57-67; C 6, L 1-4, L 18-23 – when a data request (instruction) corresponding to an asserted LP bit is paired with a data request (instruction) corresponding to an un-asserted LP bit,

a first request having an un-asserted LP bit is executed via the primary pipeline and accesses the data cache while the second request having an asserted LP bit is executed via the secondary pipeline and accessing the prefetch cache in place of the data cache); a first program counter for use when the processor operates in the normal mode (C 4, L 10-11; C 5, L 57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C 2, L 24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Regarding claim 13, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data (Lopez-Aguado - Figure 5, Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

5. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820) as applied to claims 1 and 11 above and further in view of Handy, The Cache Memory Book.

Lopez-Aguado and Shiell disclose the second data cache as an associative cache (Lopez-Aguado - C 4, L 46-50), however, Lopez-Aguado does not disclose the first cache as a direct mapped cache. Handy teaches that direct mapped caches are the simplest most common way to design a cache (Lopez-Aguado - Page 54, Paragraph 1, last two lines). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Lopez-Aguado's first cache as a direct mapped cache for the desirable purpose of simplification.

Allowable Subject Matter

6. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

August 18, 2004